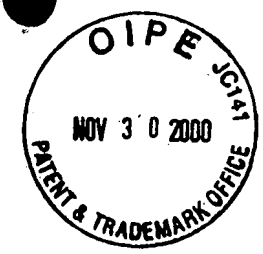
1763

TSMC-00-143



November 29, 2000

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/669,159 09/25/00

Horng-Wen Chen, Chi-How Wu

AN IN-SITU STRIP PROCESS FOR POLYSILICON ETCHING IN DEEP SUB-MICRON TECHNOLOGY

Grp. Art Unit: 1763

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,885,902 to Blasingame et al., "Integrated ARC and Polysilicon Etching Process", discloses a method to etch an anti-reflective coating (ARC) layer using an inert gaseous plasma containing helium, nitrogen, or a mixture thereof.

U.S. Patent 5,767,018 to Bell, "Method of Etching a Polysilicon Pattern", teaches a method to etch a polysilicon pattern where an anti-reflective coating (ARC) is used.

U.S. Patent 6,037,266 to Tao et al., "Method for Patterning a Polysilicon Gate with a Thin Gate Oxide in a Polysilicon Etcher", discloses a method to etch a polysilicon pattern.

U.S. Patent 5,346,586 to Keller, "Method for Selectively Etching Polysilicon to Gate Oxide Using an Insitu Ozone Photoresist Strip", teaches a method to etch a polysilicon pattern.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761